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Remarks

Thorough examination by the Examiner is noted and appreciated.

Support for the amended claims is found in the previously presented claims, the Specification and the Figures.

No new matter has been added.

For example support for the amendments and new claims is found in the Figures including Figure 1E and the Specification at:

[0004] For example, in prior art processes, a metal filled contact interconnect or via have been used to make contact from the active contact regions including gate electrode and S/D regions to the first metallization layer **through a single Interlayer-dielectric (ILD) layer, also referred to as a pre-metal dielectric (PMD) layer**. In prior art approaches, The ILD layer is formed overlying the active devices followed by formation of metal filled contacts extending through the ILD layer thickness to electrically connect the active regions **to an overlying metallization layer which begins the formation of wiring circuitry formed in multiple overlying metallization levels.**

0021 Preferably, the aspect ratio, **defined herein as the contact opening depth/ contact opening width at the bottom portion of the contact opening,** is preferably less than about 3.3 with the contact opening width at the bottom portion of the contact hole being less than about 70 nm. Thus the thickness of the first ILD layer following planarization including optional deposition of one or more of a hardmask layers and overlying

inorganic or organic anti-reflectance (ARC) coatings, is preferably less than about 2350 Angstroms to form with the preferred contact opening aspect ratio. More preferably, the aspect ratio for the contact hole formed in the first ILD layer is less than about 4.5 with a contact opening width (bottom portion) less than about 50 nm.

0023 Referring to Figure 1C, following formation of an inorganic or organic ARC layer 24B one or more resist layers e.g., 26 is deposited and patterned. The resist layer 26 may be a single or multiple layer resist including organic and inorganic materials, for example a lower organic rest layer and an overlying resist including silicon incorporated by a silylation process or including silicon monomers. The resist layer e.g., 26 may have a total thickness of about 0.1 microns to about 1.0 microns, and is preferably sensitive to wavelengths less than about 400 nm. A lithographic patterning process is carried out including radiation exposure and development by appropriate wet or dry development processes, followed by conventional dry etching processes to etch through the first ILD layer 22A to form a first set of contact openings e.g., 28A, 28B, 28C, 28D, and 28E. **The contact openings may be formed in the shape of an oval (circular), butt contact, rectangular (e.g., square), or combinations thereof.** For example, the contact openings may **include a local interconnect opening**, e.g., 28C, having the preferred aspect ratio at a lowermost (bottom) portion of the **contact opening.**

0026 Referring to FIG. 1F, a similar process as outlined for forming the first set of contact interconnects 30A, 30B, 30C, 30D, and 30E is then carried out to form a second set of contact interconnects e.g., 32A, 32B, and 32C extending through the thickness of the second ILD layer 22B to make contact (e.g., including overlying and at least partially encompassing) portions of the first set of contact interconnects. **The second set of contact interconnects is formed according to the same preferred embodiments and aspect ratios as the first set of contact interconnects the first ILD layer 22A.** The second set of contact interconnects may have the **same or different preferred aspect ratio as the second set of contact interconnects, for example having a smaller aspect ratio** to ensure adequate interconnect overlap. In addition, longer (horizontal to the substrate) contact interconnects e.g., 32A may be formed to conductively connect one or more of the first set of contact openings e.g., 30A and 30B. Preferably, the **length** of the longer contact interconnects, e.g., 32A is between about 0.15 microns and about 500 microns."

Claim Objections

The claims have been amended to overcome Examiners objections.

Claim Rejections under 35 USC 103

1. Claims 18-22, 24, 25, 27-30, 32-35, and 27-stand rejected under 35 USC Section 103(a) as being unpatentable over Tamaru (US 2003/0030146) in view of Chen et al. (6,784,096).

Tamaru disclose a single contact layer (16) with contact interconnect structures (18) penetrating the single contact layer (16). Tamaru clearly disclose forming contact holes (17) and forming metal plugs (18) in the contact holes (paragraph 0079). Tamaru then disclose forming **wiring grooves** for forming **first layer Cu wiring** (24) (also referred to in the art as a metallization layer) including a barrier layer separating the **contact metal plugs** and the **Cu wiring in metallization layers above the contact layer** (16) (see paragraphs 0080, 0087, 0088; Figures 6 and 7). Thus, in cross section the Cu **wiring** (24) overlies the **single contact layer including a contact**

interconnect structure i.e., contact plugs (18) (see also Abstract and claim 1).

Therefore Tamaru fails to disclose Applicants invention including those elements in **bold type**:
With respect to claim 18:

"A contact interconnect structure comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first plurality of metal filled contact openings extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second plurality of metal filled contact openings, each of said second plurality of metal filled contact openings extending through the second contact layer thickness to a respective one or more of the first plurality of metal contact filled openings;

wherein, the first plurality and the second plurality of metal filled contact openings **form a physically continuous contact interconnect structure**, said first and second metal filled contact openings having an aspect ratio of less than about 4.5 with respect to a respective contact layer, **said contact interconnect structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers.**"

Thus, one of ordinary skill would understand that the wiring layers of Tamaru are not part of a contact interconnect structure and the wiring grooves are not contact openings according to the plain meaning of the terms as used and taught by Tamaru.

See e.g., MPEP 2111.01:

> During examination, the claims must be interpreted as broadly as their terms reasonably allow. **This means that the words of the claim must be given their plain meaning** unless applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).
>
> When not defined by applicant in the specification, **the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art.** *In re Sneed*, 710 F.2d 1544, 218 USPQ 385 (Fed. Cir. 1983).

In contrast to Tamaru, and in non-analogous art, Chen et al.

disclose a method of **forming a barrier layer to line vias** where the **vias** are disclosed to have a width less than 70 nm or an aspect ratio greater than about 3:1 (see Abstract; Figures).

"Embodiments of the present invention provide **methods and apparatus for forming barrier layers in high aspect ratio vias (e.g., vias having aspect ratios of 3:1, 4:1, 5:1 or higher)** and/or **vias having via widths of about 0.065-0.2 microns or below**. It will be understood that the invention also may be employed to form barrier layers in lower aspect ratio and/or wider vias. Each embodiment allows a relatively thick barrier layer to be deposited on the sidewalls of a via with little or no barrier layer coverage on the bottom of the via. Adequate diffusion resistance and/or mechanical strength thereby may be provided without significantly increasing the contact resistance of the interconnect formed with the via."

Even assuming *arguendo*, a proper motivation to modify Tamaru based on the teachings of Chen et al., such modification fails to produce Applicants invention.

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir.*

1991).

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).*

2. Claims 26 and 36 stand rejected under 35 USC Section 103(a) as being unpatentable over Tamura, above in view of Chen et al., above, and further in view of Ono (IEE Trans on Electronic Devices, pg 1822 Vol. 42, No. 10, 1995).

Applicants reiterate the comments made above with respect to Tamura and Chen et al.

Even assuming *arguendo,* a proper motivation to further modify Tamura with the teachings of Ono, the further fact that Ono discloses a gate length of less than about 45 nm without a corresponding disclosure or teaching of a contact interconnect structure does not further help Examiner in producing Applicants invention.

"**First,** there must be some **suggestion or motivation,** either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)*.

Conclusion

The cited references, singly or in combination fail to produce or suggest Applicants disclosed and claimed invention, and therefore fail to make out a *prima facie* case of obviousness.

Applicants have further amended their claims and added new claims to further clarify Applicants invention. Applicants

respectfully request favorable consideration of their claims.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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